

JUN 08 2007

Application No. 10/517,591
Art Unit:Dkt. 520.44478X00
Page 2**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-18. (Canceled without prejudice or disclaimer).

19. (New) A bus system adapted to transfer data between a plurality of semiconductor devices, comprising:

a first wiring extending in a first direction from a first semiconductor device;

n-coupling wirings forming directional couplers extending in sequence away from said first semiconductor device in said first direction, each of said directional couplers being parallel to said first wiring; and

n semiconductor devices, different from the first semiconductor device, each respectively connected to a corresponding one of said directional couplers,

wherein each of the directional couplers has a predetermined coupling length and a predetermined wiring interval of spacing from the first wiring,

wherein the coupling lengths of the directional couplers decrease as the respective distance of the directional couplers from the first semiconductor device increases, and

wherein the wiring intervals of spacing of the directional couplers from the first wiring decrease as the respective distances of the directional couplers from the first semiconductor device increase.

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20. (New) A bus system according to claim 19, wherein the first semiconductor circuit is a memory controller.

21. (New) A bus system according to claim 19, wherein the n semiconductor devices are DRAMS.

22. (New) A bus system according to claim 20, wherein the n semiconductor devices are DRAMS.